WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer and including a plurality of side surfaces and a top surface;

a first gate formed on the insulating layer proximate to one of the plurality of side surfaces of the fin;

a second gate formed on the insulating layer separate from the first gate and proximate to another one of a plurality of side surfaces of the fin;

a protective layer formed above the fin, the first gate, and the second gate; and

a third gate formed over the protective layer and over the fin.

2. The semiconductor device of claim 1, further including:

first and second dielectric layers formed along the plurality of side surfaces of the fin and in contact with the first and second gates, respectively.

3. The semiconductor device of claim 1, wherein the protective layer is formed to a thickness of about 150 Å to 300 Å.

4. The semiconductor device of claim 1, wherein the third gate is formed to a thickness of about 200 Å to 1000 Å.

5. The semiconductor device of claim 1, wherein the fin comprises at least one of silicon and germanium.

6. The semiconductor device of claim 1, wherein the insulating layer comprises a buried oxide layer.

7. The semiconductor device of claim 1, further comprising:

a source region and a drain region formed above the insulating layer and adjacent a respective first and second end of the fin.

8. The semiconductor device of claim 1, wherein the first, second, and third gates are independently addressable.

9. The semiconductor device of claim 1, wherein the first and second gates are electrically connected to one another and the third gate is independently addressable from the first and second gates.

10. A method of manufacturing a semiconductor device, comprising:

forming an insulating layer on a substrate;

forming a fin structure on the insulating layer, the fin structure including a first side surface, a second side surface, and a top surface;

forming source and drain regions at ends of the fin structure;

depositing a first gate material over the fin structure, the first gate material surrounding the top surface and the first and second side surfaces;

etching the first gate material to form a first gate electrode and a second gate electrode on opposite sides of the fin structure;

planarizing the first gate material proximate to the fin structure;

depositing a protective layer above the planarized first gate material and the fin structure; and

depositing second gate material on the protective layer and above the fin structure.

11. The method of claim 10, wherein the fin structure is formed to a height of from about 300 Å to about 1000 Å.

12. The method of claim 10, wherein the planarizing includes:

polishing the first gate material so that no gate material remains above the fin structure.

13. The method of claim 10, further comprising:

growing oxide layers on the first side surface and the second side surface of the fin structure.

14. The method of claim 10, further comprising:

forming the protective layer to a thickness of about of about 150 Å to about 300 Å.

15. The method of claim 10, further comprising:

depositing the second gate material to a thickness of about 200 Å to about 1000 Å.

16. A MOSFET device comprising:

a substrate;

an insulating layer formed on the substrate;

a conductive fin formed on the insulating layer;

gate dielectric layers formed on side surfaces of the conductive fin;

a first gate material layer formed on the insulating layer and around the conductive fin;

a protective layer formed over the conductive fin and the first gate material; and

a second gate material layer formed over the protective layer and the conductive fin.

17. The MOSFET device of claim 16, wherein the MOSFET device is a FinFET.

18. The MOSFET device of claim 16, wherein the first and second gate material layers are formed of polysilicon.

19. The MOSFET device of claim 16, wherein the gate dielectric layers and the conductive fin break the first gate material layer into independently addressable first and second gates of the MOSFET device.

20. The MOSFET device of claim 19, wherein the second gate material forms a third independently addressable gate of the MOSFET device.